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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/459,995	12/14/1999	ALEX CHALFIN	15-4-833.00	1891

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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/459,995	Applicant(s) CHALFIN ET AL	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-15 have been presented for examination. Claims 1-15 have been examined and rejected.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed. The drawings filed on 12-14-1999 are acceptable subject to correction of the formalities listed in the attached "Notice of Draft person's Patent Drawing Review," PTO-948.

Claim Interpretation

3. The claims have been given the broadest interpretation by the examiner. For the purposes of examination the examiner has determined that the term *"Clock Credit"* refers to the use of a data structure that is passed from a simulation control module and different executing simulation modules for the purpose of determining how many clock cycles that particular simulation module will execute and is therefore a *Token* or *Tag* that is used to determine which simulation module is currently executing and for how many clock cycles that module will execute. For purposes of examination the examiner has determined that the term *"test bench"* refers to the set of test signals that are used as inputs to stimulate a circuit under simulation testing. For purposes of examination the examiner has determined that the term *Clock arbitrator* is any type of Master Clock or Central Control module that controls the distribution of clock signals throughout a simulation module.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-5, 11, 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth et al. U.S. Patent 5,732,247** in view of **Flynn U.S. Patent 5,790,829** and in further view of **Okuda U.S. Patent 5,363,319** and in further view of **Microsoft Press Computer Dictionary, Third Edition, *Published 1997*** here after referred to as the *Microsoft* reference.

As regards **Claims 1 and 11,** the *Dearth et al.* reference discloses, a method of synchronizing a plurality of simulation modules **(Figure 1 and Col. 2 Lines 21-62, Col. 13 Lines 15-35, Col. 19 Lines 13-14);** ***(a)*** initializing a simulation module **(Figure 4a-d, and Col. 5 Lines 17-27, Col. 6 Lines 54-57, Col. 15 Lines 25-37),** by sending a MSG packet **(Figure 2),** ***(b)*** execution corresponding to an extent determined by the reception of a packet from the Comm Interface Core **(Figure 1 Items 20,21 and 23), (Figure 3, Figure 4C Item 115 and Col. 4 Lines 32-49, Col. 5 Lines 8-40),** ***(c)*** halting execution when the testing for that simulation module has been completed **(Figure 3 Items 61, 62, 63, Figure 4A Item 108, Figure 4B Item 109 and Col. 2 Lines 20-63, Col. 5 Lines 40-49),** ***(d)*** when additional processing by at least one simulation module s necessary, issuing a further MSG packet to each simulation module, **(Figure 3 Item 64**

and Figure 4C and Figure 4D Item 121 and Col. 4 Lines 32-49, Col. 5 Lines 40-57, Col. 8 Lines 32-39, Col. 9 Lines 24-44).

The *Dearth et al.* reference does not expressly disclose issuing a *Clock Credit* or *Token* to control the different simulation modules, although the MSG packet disclosed in **Figure 2** of the *Dearth et al.* reference effectively performs some of the functions of a control Token, *i.e. the transfer of control information.*

The *Flynn* reference discloses the use of a Token to control module execution **(Figures 2-12 and Col. 3 Lines 15-61).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the *Dearth et al.* reference with the *Flynn* reference because, *(motivation to combine)*,**(Col. 3 Lines 62-63 of the *Flynn* reference),** The use of Tag events to synchronize processing of families of events enables effective synchronization of simulation of the events of the family.

As regards **Claims 2 and 12** the *Dearth et al.* reference discloses synchronization points identified in data passing between the simulation modules **(Figure 2 Items 41-46 and Figure 4B Item 109 and all of Figures 4C-D and Col. 2 Lines 21-63, Col. 4 Lines 24-28, Col. 6 Lines 54-58).**

As regards **Claims 3 and 13** the *Dearth et al.* reference does not expressly disclose the creation of a Master Clock signal, nor dividing the Master Clock signal to derive an additional clock signal, nor applying the additional clock signal to a plurality of simulation modules.

The *Okuda* reference discloses, the creation of a Master Clock signal **(Figure 4 Item 43)** dividing the Master Clock signal to derive an additional clock signal **(Figure 4 Items 35, 45, 201**

and Figure 85 and Figure 89B and Col. 35 Lines 42-68, Col. 36 Lines 1-19, Col. 36 Lines 32-51, Col. 36 Lines 52-68, Col. 37 Lines 46-68, Col. 38 Lines 31-57, Col. 39 Lines 51-68, Col. 40 Lines 1-2 and Col. 42 Lines 57-68).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the *Dearth et al.* reference with the *Okuda* reference because, *(motivation to combine), (Okuda Col. 3 Lines 35-39, ...to provide a logic simulator which can improve simulation speed by parallel operation and carry out good simulation of logic circuits even if the circuit scale is considerably large).*

As regards **Claims 4 and 5** the *Dearth et al.* reference teaches a *Test Bench* **(Figure 1 Items 11, 30, 31 and 32 and Figure 4 A-D and Col. 1 Lines 1-68, Col. 2 Lines 1-68, Col. 3 Lines 1-68, Col. 4 Lines 1-68, Col. 5 Lines 1-68 and Col. 6 Lines 1-63).**

As regards the limitation in **Claim 11** concerning the use of computer readable executable code, the *Microsoft* reference discloses computer readable code being executed from a computer readable medium **(Pages 81, 82, 145, 146, 182 183, 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Microsoft* reference because storing and executing software programs from computer readable media eliminates the requirement to manually enter the software program instructions every time a computer user wishes to execute the method described in Applicants application.

5. **Claims 6, 7, 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya U.S. Patent 5,905,883** in view of **Eirikasson U.S. Patent 5,081,601** and in further view

of **Microsoft Press Computer Dictionary, Third Edition,** ***Published 1997*** here after referred to as the *Microsoft* reference.

As regards **Claims 6 and 14** the *Kasuya* reference discloses, creating a test bench component of a simulation module comprising the steps of reading specification information, identifying the DUT, determining the interface to the DUT, **(Figure 1 Item 130 and Figure 2 and Col. 1 Lines 1-67, Col. 2 Lines 1-67, Col. 3 Lines 1-67, Col. 4 Lines 59-67 and Col. 5 Lines 1-64).**

The *Kasuya* reference does not expressly disclose supporting testing of a plurality of time domains.

The *Eirikasson* reference discloses a plurality of time domains **(Figure(s) 1-6 and Col. 4 Lines 13-30).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Kasuya* reference with the *Eirikasson* reference because, *(motivation to combine) by synchronizing two independently clocked simulators peak performance is maintained* ***(Eirikasson reference Col. 3 Lines 58-67 and Col. 4 Lines 1-30).***

As regards **Claims 7 and 15** the *Kasuya* reference discloses determining the inputs and outputs of the DUT, ascertaining the attributes of said inputs and outputs and deriving the protocols of said inputs and outputs **(Figures 1-4 and Col. 1 Lines 53-65).**

As regards **Claim 14** the *Microsoft* reference discloses computer readable code being executed from a computer readable medium **(Pages 81, 82, 145, 146, 182 183, 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Kasuya* reference with the *Microsoft* reference because storing and

executing software programs from computer readable media eliminates the requirement to manually enter the software program instructions every time a computer user wishes to execute the method described in Applicants application.

6. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Velasco et al. U.S. Patent 6,115,823** in view of **Dearth et al. U.S. Patent 5,848,236** and in further view of **"VHDL for Programmable Logic", by Kevin Skahill** *hereafter referred to as the Skahill reference,* and in further view of **Kurosawa et al. U.S. Patent 5,603,015.**

As regards **Claim 8**, the *Velasco et al.* reference discloses the use of a clock arbitrator to synchronize several computer sub-system modules **(Figure 1 Item 25 and Figure 2 Item 130, 53a, 53n and Figure 3 and Figure 11 all of Item 130 and all of Figure 12 and Figure 21 Items 248 and 249 and the rest of Figure 21 and Figure 26 and 27 and Figure 30 and all of Figure 47 and Col. 25 Lines 25-67, Col. 32 Lines 18-48, Col. 33 Lines 34-40, Col. 42 Lines 26-65).**

The *Velasco et al.* reference does not expressly disclose: synchronizing a plurality of simulation modules, a programming language interface, a test bench or a device under test.

The *Dearth et al.* reference discloses synchronizing multiple simulation modules **(Figures 1-20 and Col. 2 Lines 20-60).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Dearth et al.* reference because, *...the invention provides structure and method for a modular bus architecture (MBA) and fast modular*

bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time.(Velasco et al. Col. 4 Lines 49-54).

The *Skahill* reference discloses a programmable language interface, a test bench and a device under test **(Skahill, Pages 541-543 and Figure 10-1).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Skahill* reference because, *...the invention provides structure and method for a modular bus architecture (MBA) and fast modular bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time.(Velasco et al. Col. 4 Lines 49-54).*

As regards **Claim 9** the *Velasco et al.* reference does not expressly disclose a shared memory interface.

The *Kurosawa et al.* reference discloses a shared memory interface **(Figures 1-2 and 4a-d, and 7-17 and 25-26 and Col. 20 Lines 54-56).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Kurosawa et al.* reference because, *...the invention provides structure and method for a modular bus architecture (MBA) and fast modular bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease design time.(Velasco et al. Col. 4 Lines 49-54).*

As regards **Claim 10** the *Velasco et al.* reference does not expressly disclose having the test bench and the device under test compiled together into one executable file.

The *Skahill* reference discloses having the test bench and the device under test compiled together into one executable file. **(Skahill, Pages 541-543 and Figure 10-1).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Velasco et al.* reference with the *Skahill* reference because, ...*the invention provides structure and method for a modular bus architecture (MBA) and fast modular bus archetechure (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that* ***decrease design time****.* ***(Velasco et al. Col. 4 Lines 49-54).***

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
December 8, 2002

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